

FIG.1

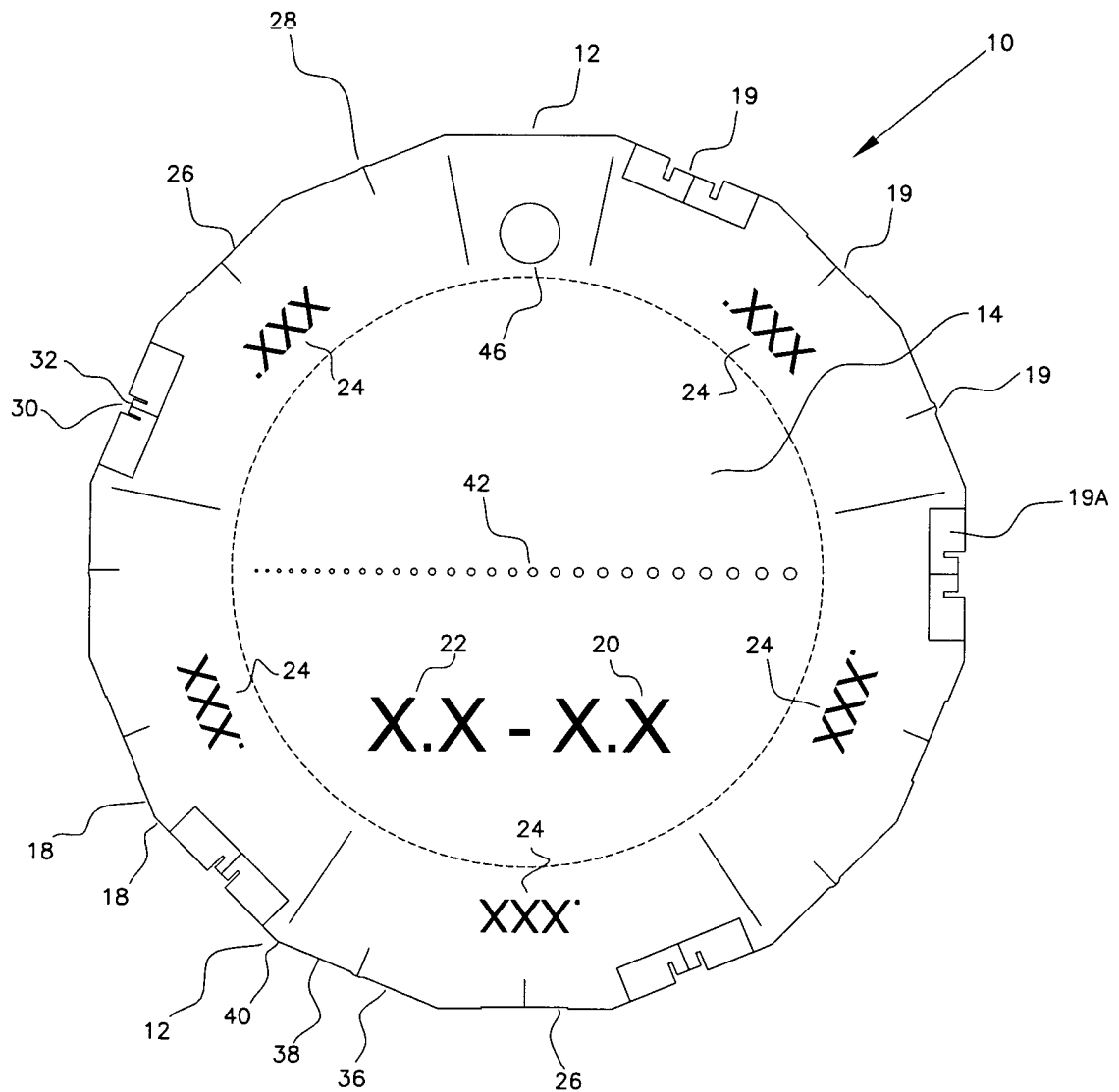


FIG.2

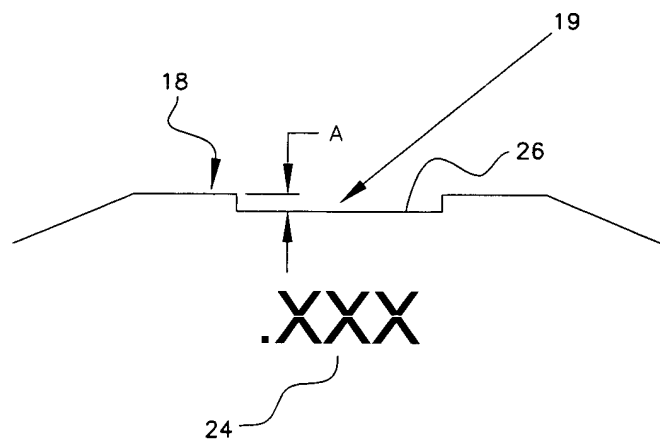


FIG.3

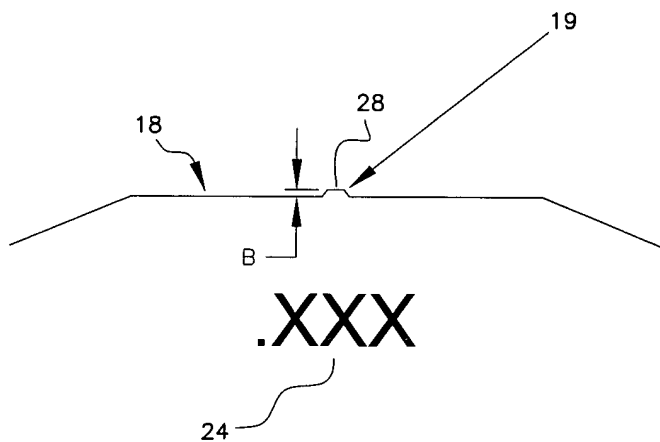


FIG.4

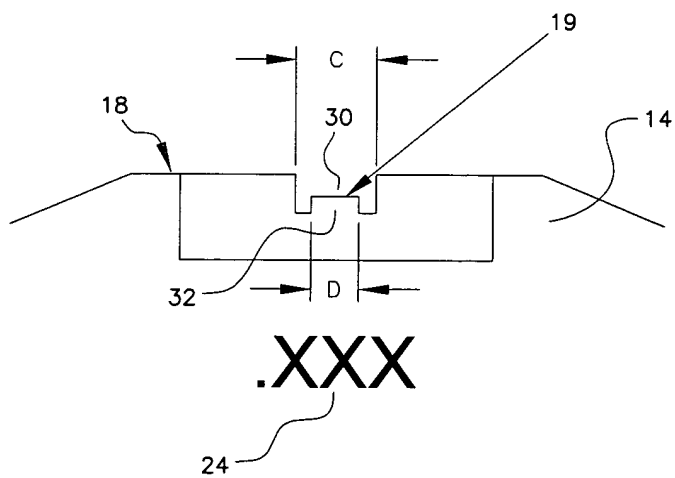


FIG. 4A

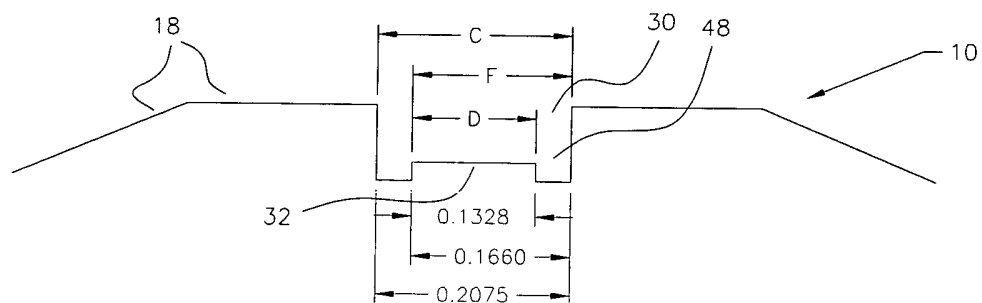


FIG. 4B

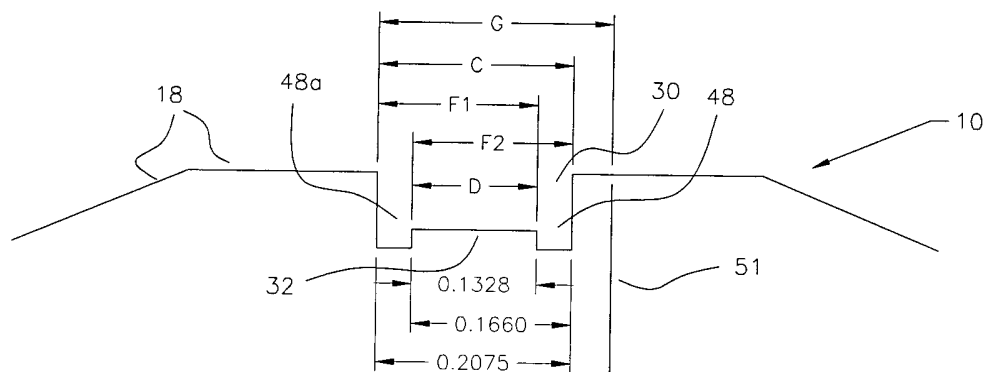


FIG. 5

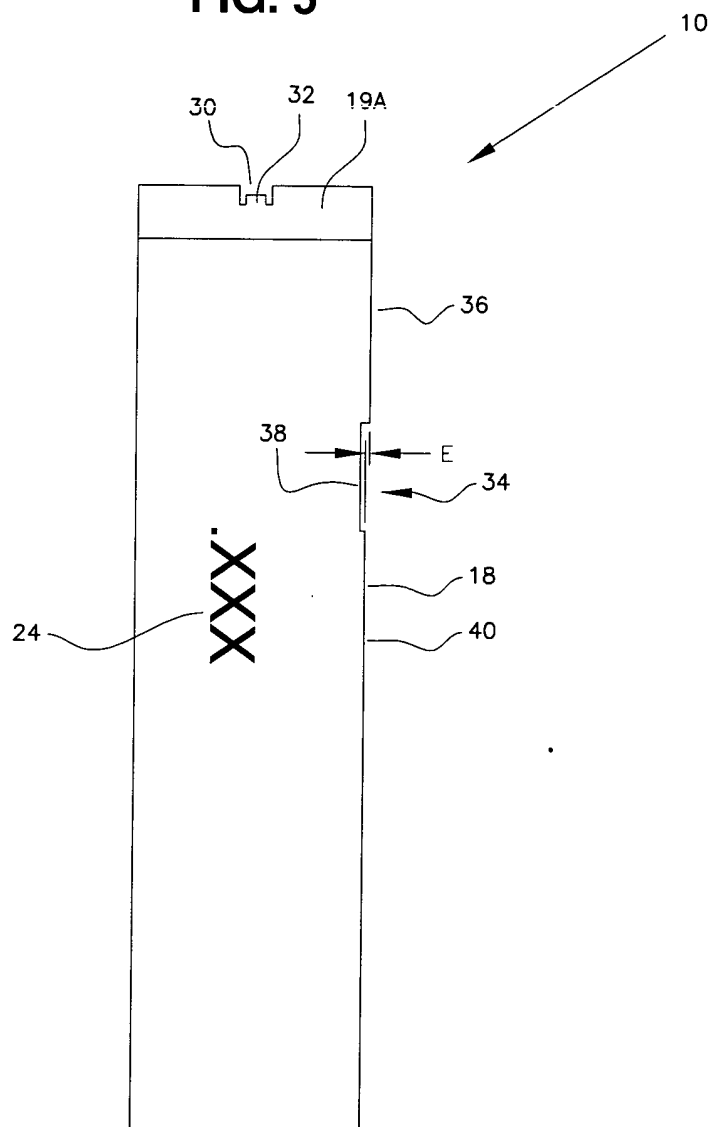


FIG. 6

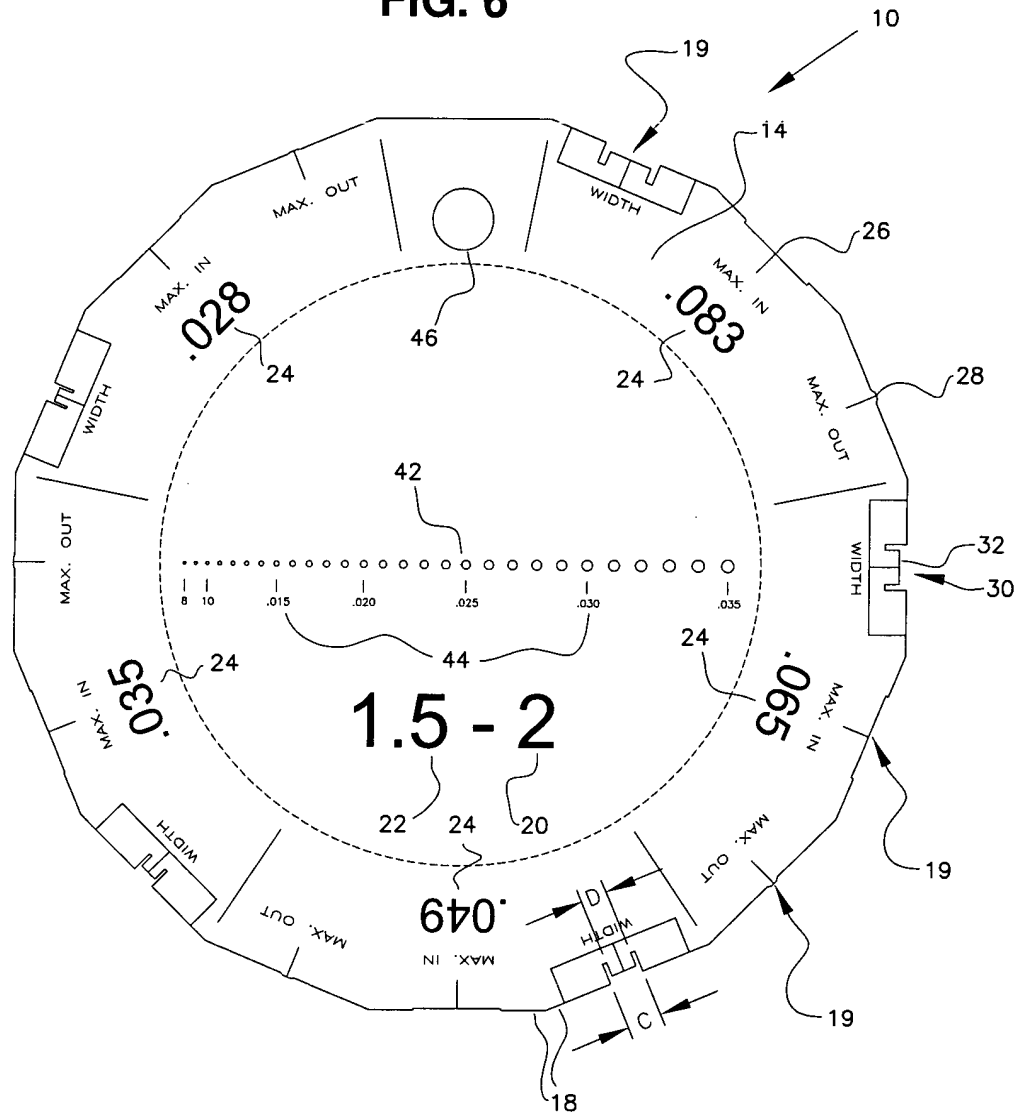


FIG. 7A

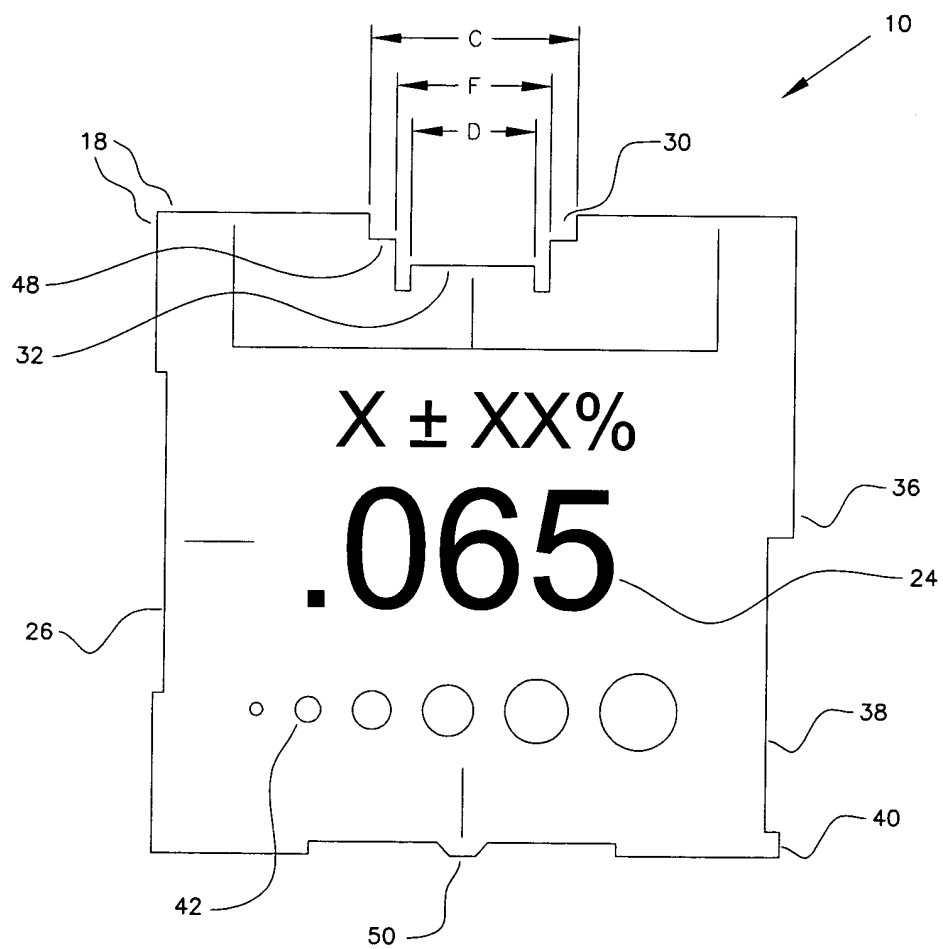


FIG. 7

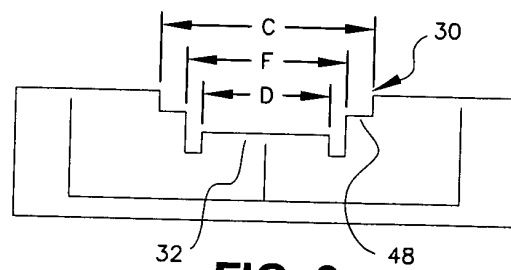
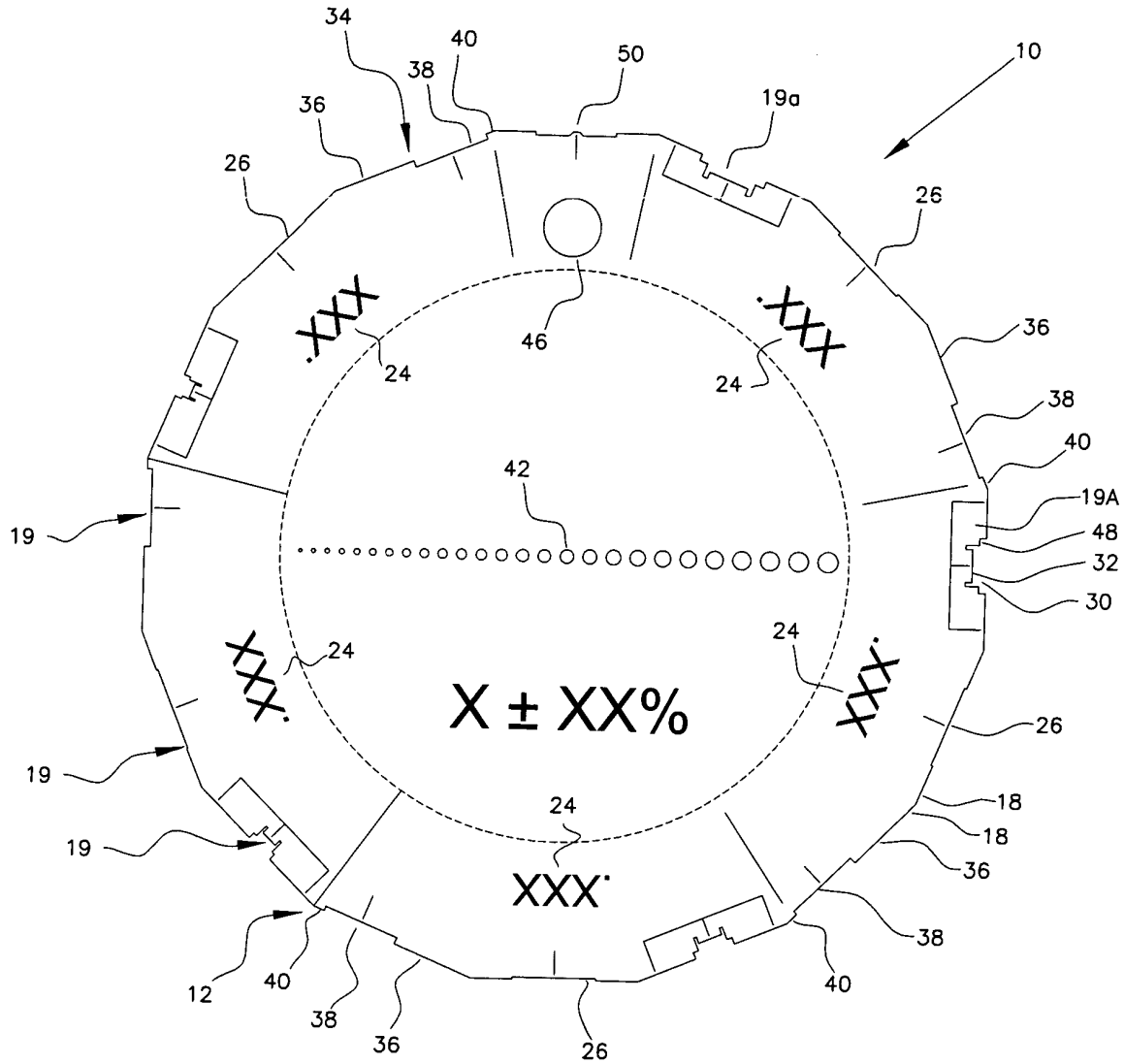


FIG. 8

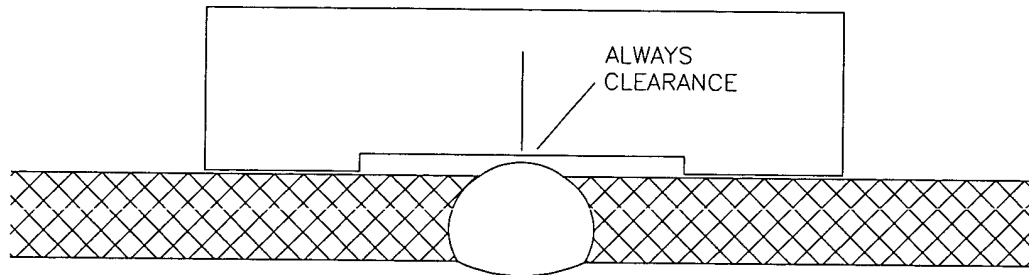


FIG. 9A

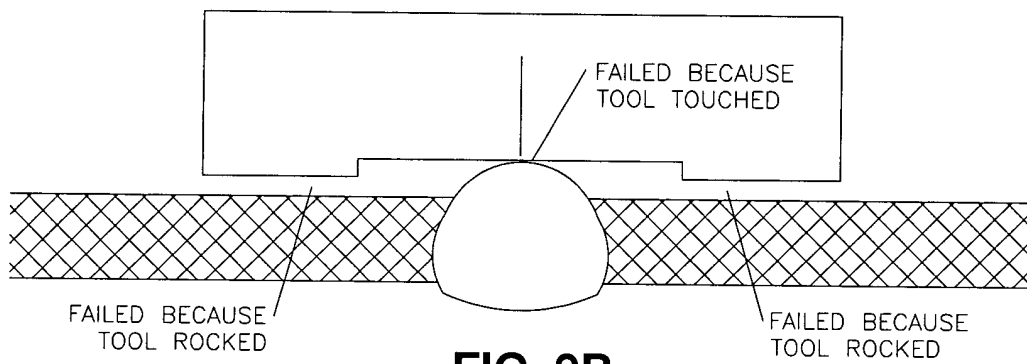


FIG. 9B

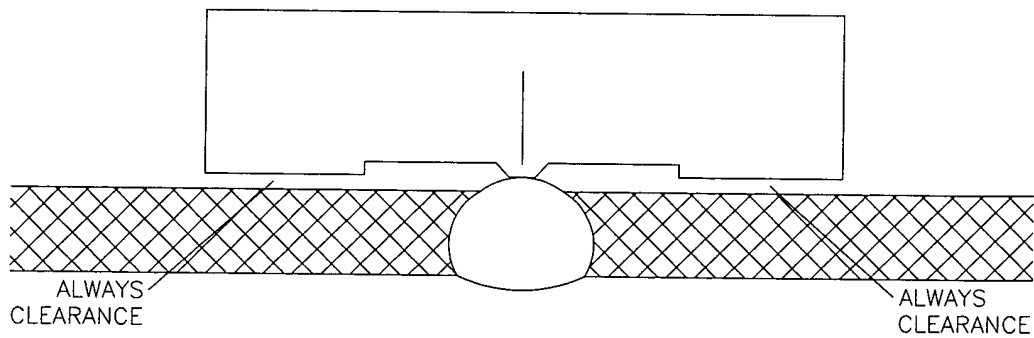


FIG. 10A

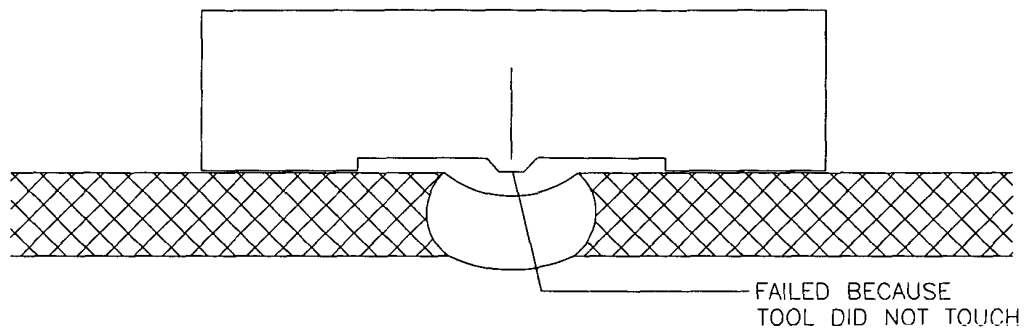


FIG. 10B

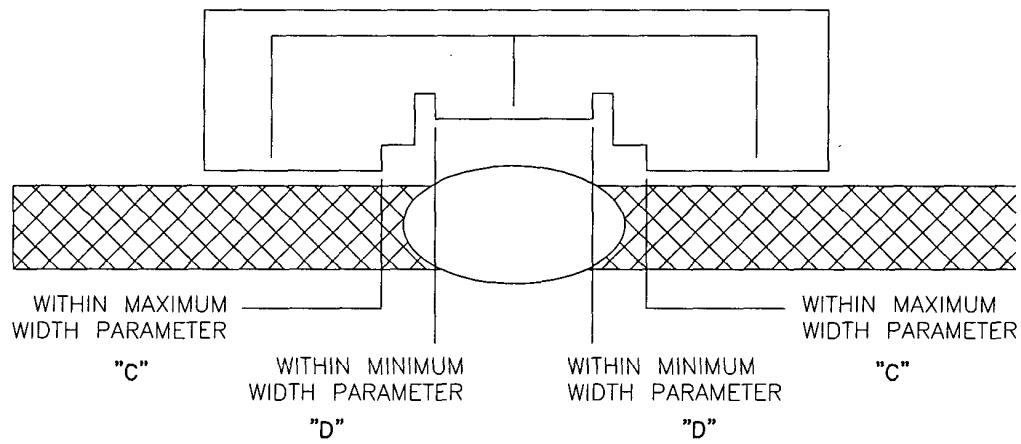


FIG. 11A

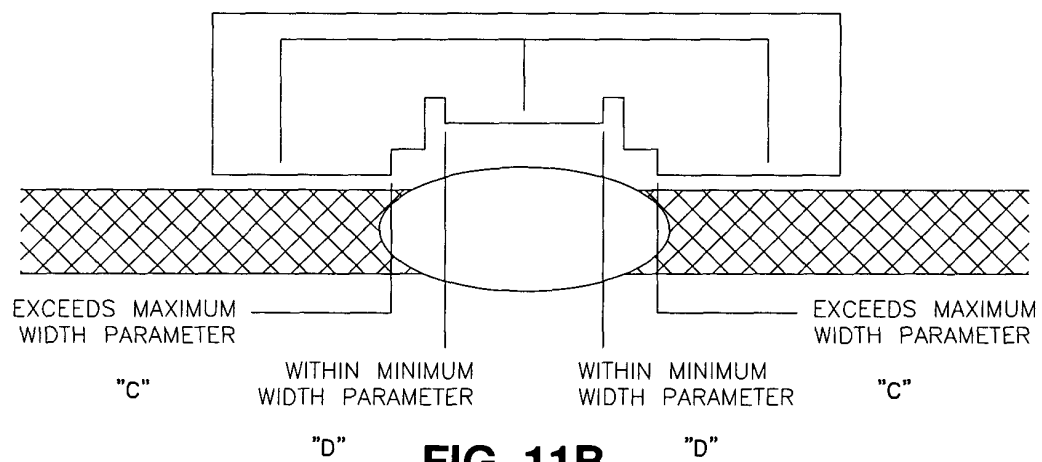


FIG. 11B

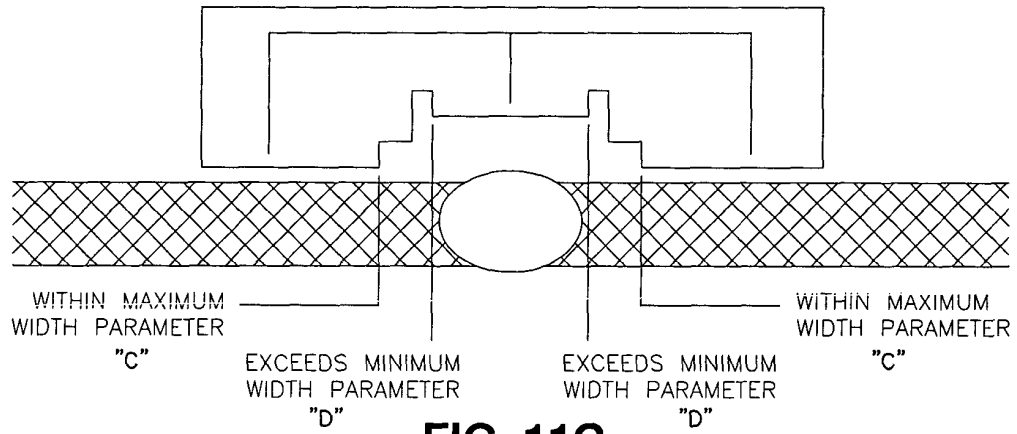


FIG. 11C

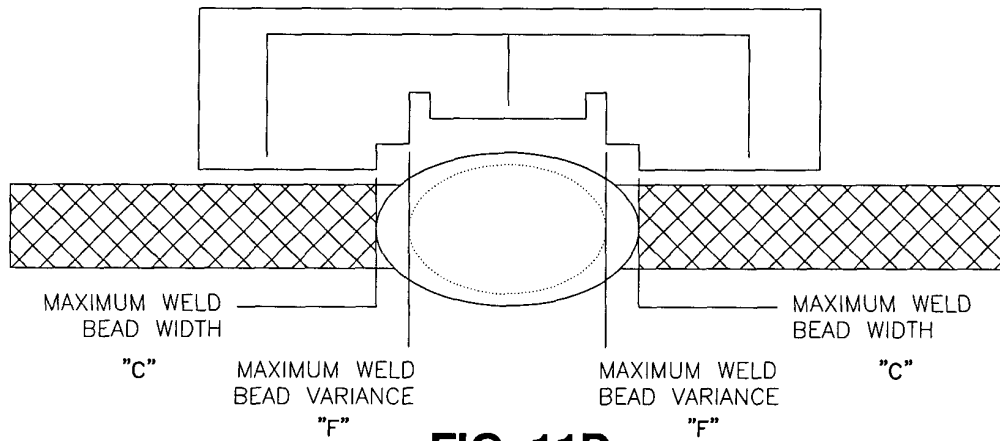


FIG. 11D

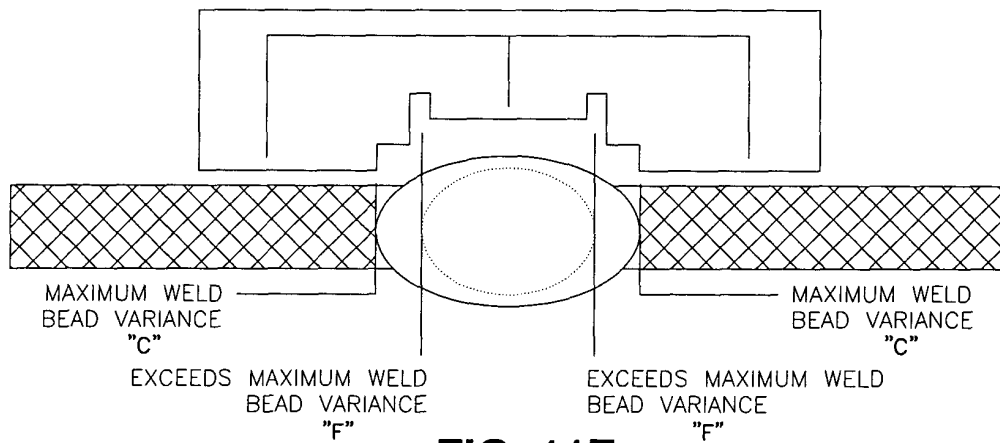


FIG. 11E

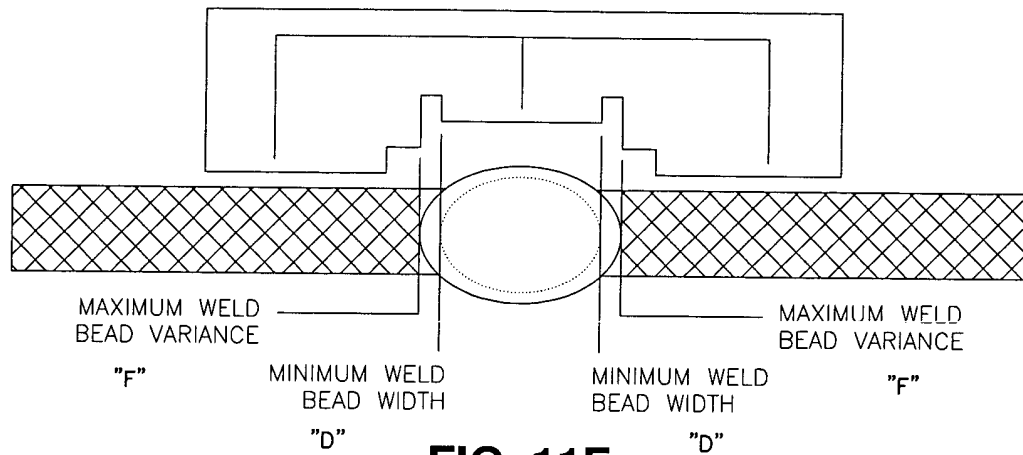


FIG. 11F

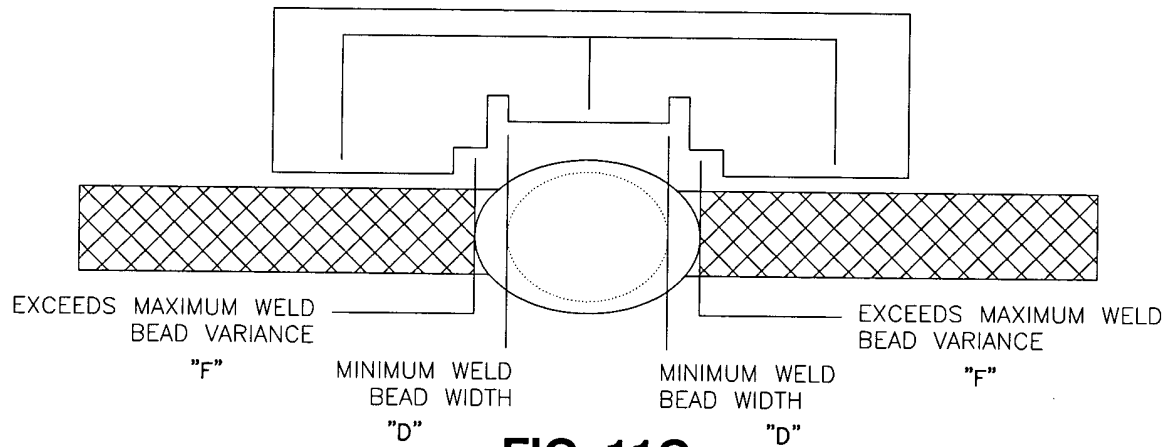
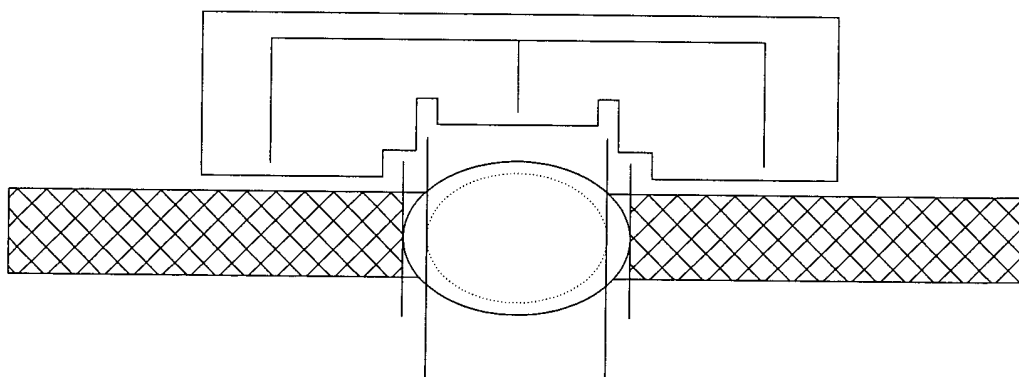


FIG. 11G



VISUAL REFERENCE OF ACCEPTANCE WITHIN MAXIMUM VARIATION OF WELD BEAD

FIG. 11H

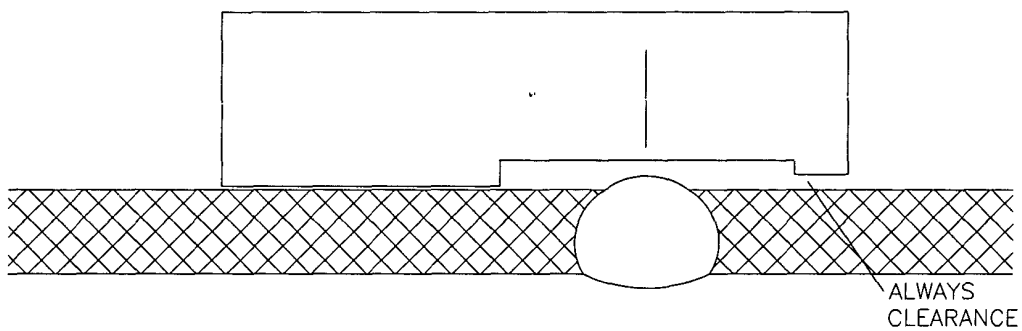


FIG. 12A

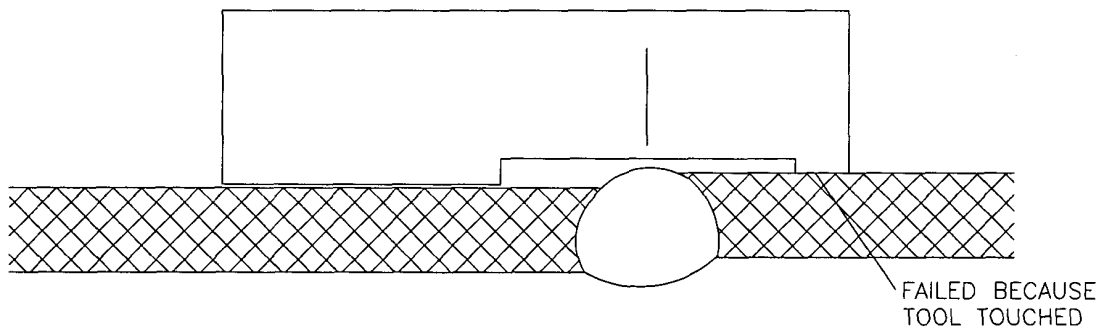


FIG. 12B

FIG. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 10 with a top layer 18. A central region 30 is defined by a series of nested rectangular structures. The outermost structure is 48a, followed by 48b, and then 48c. The central region 30 is further defined by dimensions G, C, C1, D1, and D. The substrate 10 is shown with a cross-section 51. The device is labeled with various dimensions: 0.0830, 0.1040, 0.1660, and 0.2490. The device is also labeled with 32 and 30.

FIG. 14A

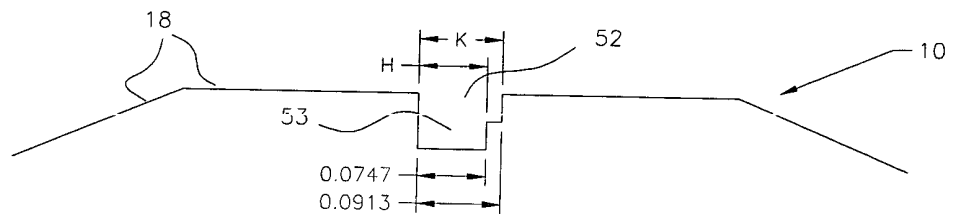


FIG. 14B

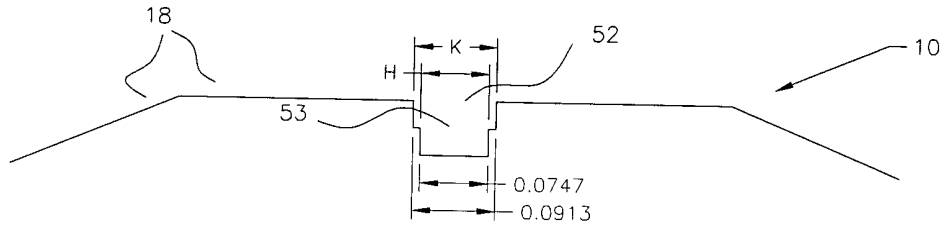


FIG. 15

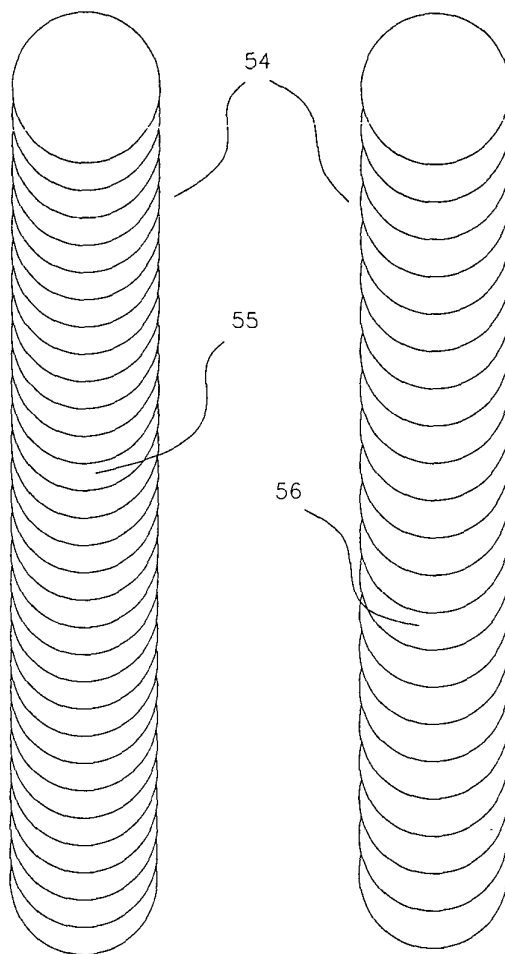


FIG. 16A

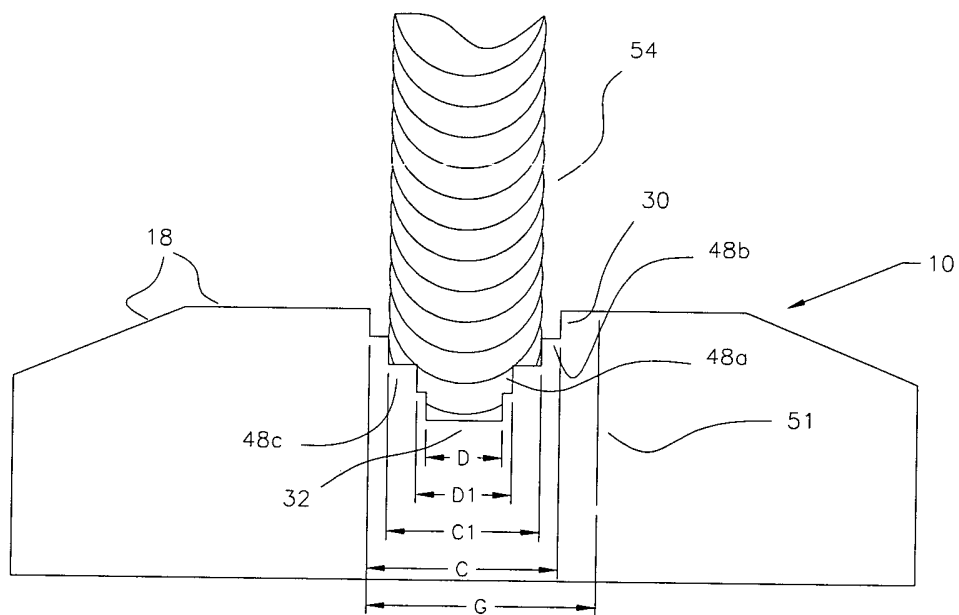


FIG. 16B

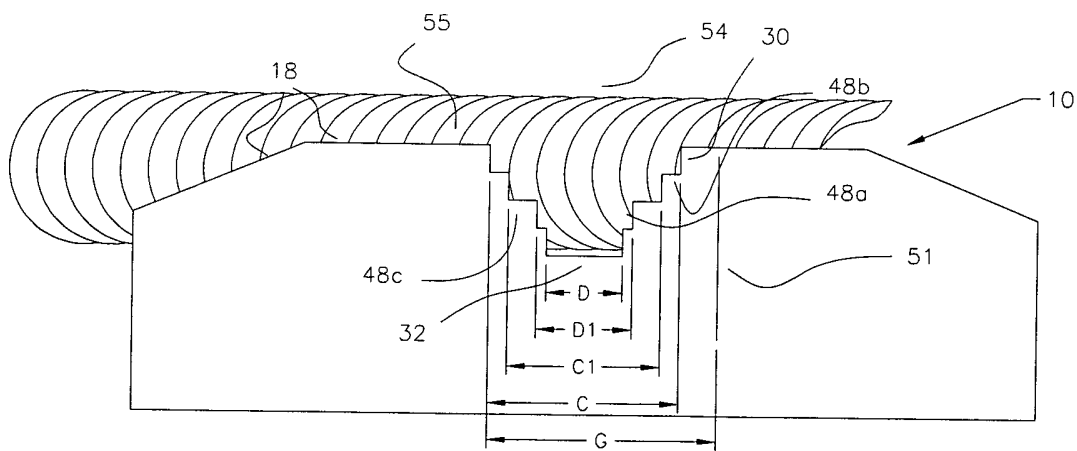


FIG. 16C

